Amendments to the Claims:

1 - 17. (Canceled)

18. (Currently Amended) ~~The device of Claim 15 or 16~~ A device for matching patterns against data comprising:

a first memory in which a set of patterns are stored;

a second memory that stores mask data identifying patterns in the first memory to be matched against the data; and

pattern match logic circuit arrangement correlating marked patterns in said first memory against the data and generating at least one control signal if a match occurs wherein the pattern match logic circuit arrangement includes a first state machine for assembling data received from a network into predetermined sizes and identifying beginnings and endings of data frames; and

a second state machine operatively coupled to the first state machine, said second state machine including circuit that receives the predetermined sizes from the first state machine and circuit that generates addresses for accessing the first memory and the second memory, whereat pattern and mask data are to be read and used with the predetermined sizes in generating the first control signal.

19 - 20. (Canceled)

21. (Previously Presented) A network interface card including:
a system interface circuit arrangement;
a network interface circuit arrangement;
a first storage that stores a set of patterns;
a second storage that stores mask data identifying patterns in the first storage to be matched against data; and
a pattern match logic circuit arrangement correlating marked patterns in said first storage with the data and generating at least one first control signal if a match occurs between one of the marked patterns and the data.

22. (Previously Presented) The network interface card of Claim 21 wherein the data is received from the network.

23. (Previously Presented) The network interface card of claims 21 or 22 further including a host computer coupled to the system interface, said host computer including software for downloading to the network interface card the set of patterns and the mask data.

24. (Previously Presented) The network interface card of claims 21 or 22 further including address match function logic circuit for correlating an address for the network interface card and a received address and generating a second control signal on the occurrence of a match.

25. (Previously Presented) The network interface card of claims 21 or 22 wherein each pattern in the set of patterns are arranged in 4 (four) bytes wide words and 128 byte sectors.

26. (Previously Presented) The network interface card of claim 25 wherein the patterns are arranged contiguously in the Pattern Storage.

27. (Previously Presented) The network interface card of claim 25 wherein the mask data is arranged so that each M-bits word of mask contains mask bits for words in N patterns, wherein M=number of bits in a mask word and N=number of patterns.

28. (Previously Presented) The network interface card of claim 27 wherein M = 32 and N = 8.

29. (Previously Presented) The network interface card of claim 21 wherein the pattern match logic circuit arrangement includes a first state machine for assembling data received from the network interface circuit arrangement into predetermined sizes and identifying beginnings and endings of data frames; and

a second state machine operatively coupled to the first state machine, said second state machine including circuit that receives the predetermined sizes from the first state machine and circuit that generates addresses for accessing the pattern storage and mask storage, whereat data are to be read and used with the predetermined sizes in generating the first control signal.

30. (Previously Presented) The network interface card of claim 29 wherein the address generation circuit uses the expression YYYxxxxx to determine the addresses for the Pattern RAM, wherein xxxxx represents an index count and YYY represents states for a state machine.

31. (Previously Presented) The network interface card of claim 21 wherein the system interface circuit arrangement includes a PCI Interface.

32. (Previously Presented) The network interface of claim 21 wherein the network interface circuit arrangement includes Ethernet MII Interface.

33. (Canceled)

34. (Previously Presented) A method for using in a communications network to wake station connected to the communications network said method including the steps of:

(a) providing, on a network interface card, multiple patterns against which data from the communications network is to be matched;

(b) providing mask data indicating the patterns to be used;

(c) correlating each identified pattern with data received from the communications network; and

(d) generating a Wake-Up signal if a match occurs in step (c).

35. (Previously Presented) The method of claim 34 further including the steps of

(e) a receiving station correlating a station address with an address received with the data from the communications network; and

(f) generating the Wake-Up signal only if a match occurs in step e and a match occurs in step c.

36. (Currently Amended) ~~The method of claim 33 wherein the pointers include~~ A pattern matching method including the steps of:

(a) providing a set of patterns;

(b) providing data to be matched with selected patterns in said set of patterns;

(c) providing pointers including mask bits.

37. (Previously Presented) The method of claim 36 wherein the set includes eight patterns.

38. (Previously Presented) The method of claim 37 wherein the mask bits includes 32 bits with groups of 4 mask bits identifying one of the eight patterns.

39. (New) A device for matching patterns against data comprising:

a first memory in which a set of patterns are stored;

a second memory that stores mask data identifying patterns in the first memory to be matched against the data; and

pattern match logic circuit arrangement correlating marked patterns which are fewer than the total number of patterns in said first memory, wherein the pattern match logic circuit arrangement includes a first state machine for assembling data received from a network into predetermined sizes and identifying beginnings and endings of data frames; and

a second state machine operatively coupled to the first state machine, said second state machine including circuit that receives the predetermined sizes from the first state machine and circuit that generates addresses for accessing the first memory and the second memory, whereat pattern and mask data are to be read and used with the predetermined sizes in generating the first control signal.